SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2008-267592, filed on Oct. 16, 2008; the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] This invention relates to a semiconductor device used in power control.

[0004] 2. Background Art

[0005] The ON resistance of a vertical power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) greatly depends on the electrical resistance of the conduction layer (drift layer). The impurity concentration that determines the electrical resistance of the drift layer cannot be increased above a limit according to the breakdown voltage of the p-n junction formed by the base layer and the drift layer. Therefore, a tradeoff relationship exists between the device breakdown voltage and the ON resistance. It is important to improve this tradeoff in devices of low power consumption. The tradeoff includes a limit determined by the device material. Overcoming this limit leads to the realization of a low ON resistance device superior to existing power devices.

[0006] To solve these problems, a known example of a MOSFET includes a p-type pillar layer and an n-type pillar layer buried in the drift layer in a structure called a super junction structure. The super junction structure has the same amount of charge (impurity amount) in the p-type pillar layer and the n-type pillar layer and thereby creates a pseudo-non-doped layer, holds a high breakdown voltage, and passes a current through the highly doped n-type pillar layer to realize a low ON resistance superior to that of the material limit. Thus, the tradeoff between the ON resistance and the breakdown voltage superior to those of the material limit is possible to be achieved based on the super junction structure.

[0007] When the power MOSFET is used for a bridge circuit and synchronous rectification or the like, a built-in diode may be operated. Usually, bipolar operation is necessary for large current operation of the diode with low ON voltage. However, if the ON resistance is reduced by using the MOSFET having the super junction structure, the low ON voltage can be achieved in spite of unipolar operation of the built-in diode.

[0008] For example, JP-A 2007-299970 (Kokai) discloses a structure of a MOSFET having a built-in Schottky barrier diode (a structure having a MOSFET and a Schottky barrier diode mixed loaded on one chip). However, a region serving as the MOSFET and a region serving as the Schottky barrier diode are formed separately in one chip, causing concern about reducing an effective area of the MOSFET to increase the ON resistance.

SUMMARY OF THE INVENTION

[0009] According to an aspect of the invention, there is provided a semiconductor device including: a first semiconductor layer of a first conductivity type; a second semiconductor layer of a first conductivity type provided on a major surface of the first semiconductor layer; a third semiconductor layer of a second conductivity type provided above the major surface of the first semiconductor layer adjacent to the second semiconductor layer, and forming a periodical arrangement structure in conjunction with the second semiconductor layer in a lateral direction generally parallel to the major surface of the first semiconductor layer; a fourth semiconductor layer of a second conductivity type provided on the third semiconductor layer; a fifth semiconductor layer of a first conductivity type selectively provided on a surface of the fourth semiconductor layer; a first main electrode electrically connected to the first semiconductor layer; a gate insulating film provided on a portion being in contact with the fourth semiconductor layer, a portion being in contact with the fifth semiconductor layer and a portion being in contact with the second semiconductor layer; a control electrode provided opposed to the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer through the gate insulating film; and a second main electrode electrically connected to the fourth semiconductor layer, the fifth semiconductor layer and the second semiconductor layer, the second main electrode being in contact with a surface of the second semiconductor layer located between the control electrodes to form a Schottky junction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGS. **1** and **2** are cross-sectional views of main components of a semiconductor device according to a first embodiment of the invention;

[0011] FIG. **3** is a cross-sectional view of main components of a semiconductor device according to a second embodiment of the invention;

[0012] FIG. **4** is a perspective view of main components of the semiconductor device according to the second embodiment of the invention;

[0013] FIGS. **5** and **6** are cross-sectional views of main components of the semiconductor device according to the second embodiment of the invention;

[0014] FIGS. **7** and **8** are cross-sectional views of main components of a semiconductor device according to a third embodiment of the invention;

[0015] FIGS. **9** and **10** are cross-sectional views of main components of a semiconductor device according to a fourth embodiment of the invention;

[0016] FIGS. **11** and **12** are cross-sectional views of main components of a semiconductor device according to a fifth embodiment of the invention;

[0017] FIG. **13** is a cross-sectional view of main components of a semiconductor device according to the fifth embodiment of the invention;

[0018] FIG. **14** is a cross-sectional view of main components of a conventional semiconductor device; and

[0019] FIG. **15** is a cross-sectional view of main components of another conventional semiconductor device.

DETAILED DESCRIPTION OF THE INVENTION

[0020] Embodiments of the present invention will now be described with reference to the drawings. In the embodiments below, a first conductivity type is assumed to be an n-type, and a second conductivity type is assumed to be a p-type. Like elements in the drawings are marked with like reference numerals.

First Embodiment

[0021] FIG. **1** is a schematic view showing a cross-section of main components of a semiconductor device according to a first embodiment of the invention.